Production-Ready, Flux-free Bump Reflow System With Activated Hydrogen

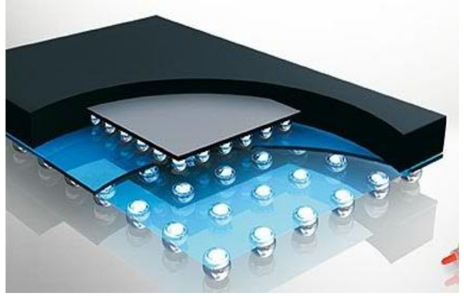
Air Products and Chemicals, Inc.
Sikama International, Inc.

Outline

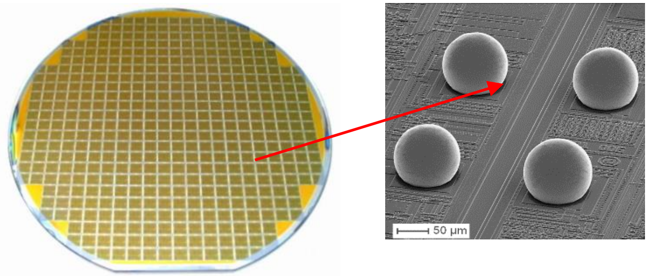
- Introduction
- System overview
- Mechanical sample results
- Electrical sample results
- System production readiness
- Hydrogen safety
- Conclusion

Wafer Bump Reflow

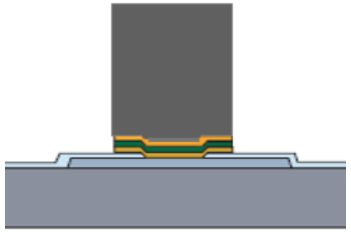
- **Packaging technology for electronics devices has advanced rapidly in recent years driven by**
  - Feature size reduction
  - New materials developed
  - Increased device functionality/reliability
  - Cost reduction
  - Environmental consideration



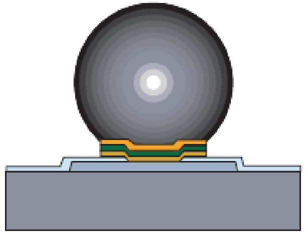
- **The most fundamental among the advanced packaging technology is the use of wafer bumping and wafer-level chip-scale packaging**
- **Our current flux free technology platform is related to wafer bumping process: wafer bump reflow and copper pillar reflow**



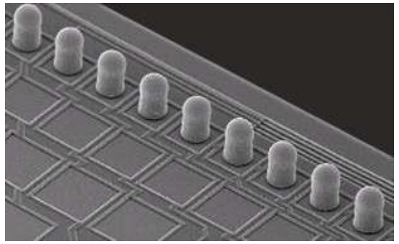
Solder bumps are formed over an entire wafer



Electroplated bump



Reflowed bump



Reflowed copper pillar

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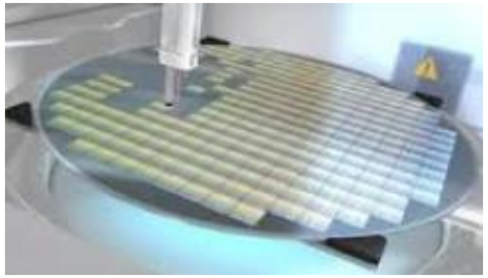
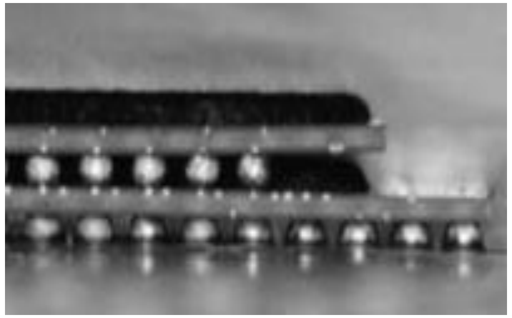
Key Requirement: Surface Oxide Removal

- **The reflowed wafer is cut into individual chips, which then go through subsequent packaging processes**
- **In the packaged devices, the formed bumps serve as electrical and mechanical connections**
- **One of the keys for successful wafer bump reflow is to ensure an oxide-free molten solder surface**
  - Any oxide layer acts as a solid skin to constrain molten solder's flow, thus affecting bump appearance and shape conversion
  - The oxide reduction is more critical and difficult as the size decreases

Single chips



Solder connections



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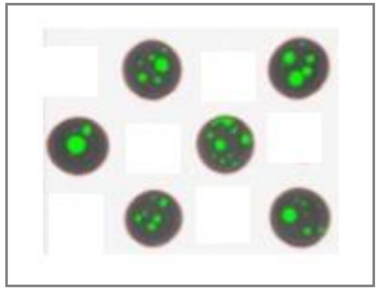
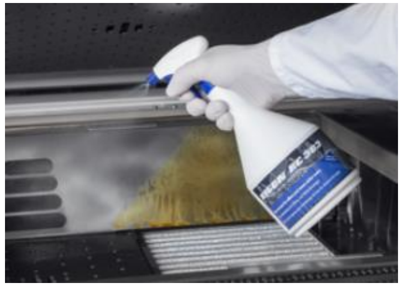
Conventional Flux-based Oxide Removal

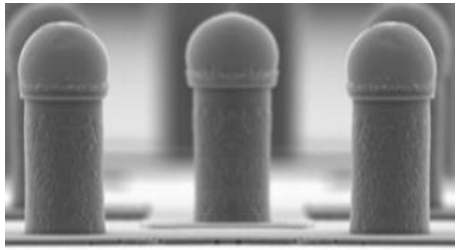
- **Process of record for eliminating solder oxides is by coating wafers with a flux and then reflow in N_2 and has issues:**
  - **Flux volatiles**
    - Void formation in solder bumps, thus degrading solder joint properties
    - Flux volatiles condense on the furnace walls, thus causing frequent maintenance for cleaning and production downtime
    - Exposure to flux fumes
  - **Flux residues**
    - Residue contaminations on wafer surface, thus requiring a post cleaning
    - Challenges for post cleaning of fine pitch and high-aspect ratio bumps and copper pillars
    - Hazardous wastes
- **Flux-free process is strongly preferred**



Voids inside solder bumps



Furnace cleaning



Copper pillar bumps

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Flux-free Methods to Remove Metal Oxide

- **Known flux-free technologies have limitations**
  - **Formic acid vapor**
    - Is not completely residue free
    - Requires bubbler system to introduce formic acid
    - Vacuum based chamber system for oxide removal
  - **H_2 or forming gas**
    - Requires temperatures ≥ 350°C for thermal activation of H_2 molecules
    - Requires flammable H_2 concentrations (≥ 5 vol%) to hasten the oxide reduction
  - **Plasma-activated H_2**
    - Is not effective at atmospheric pressure
    - Needs to be operated in vacuum, resulting in a batch process

Atmospheric plasma (DBD)

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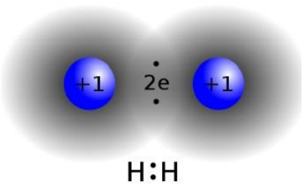
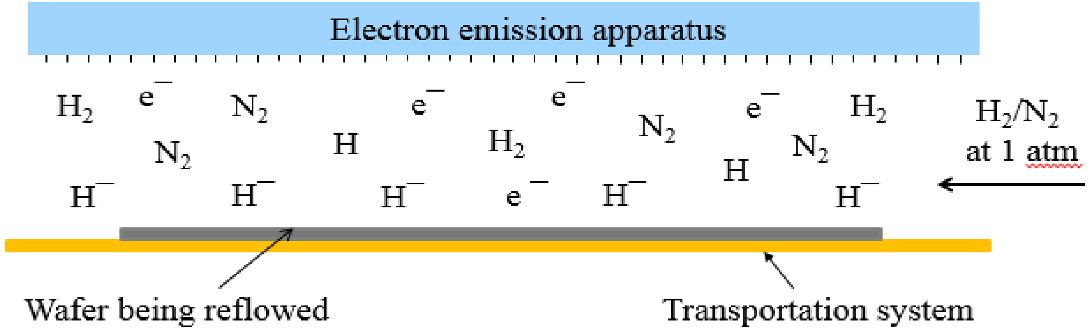
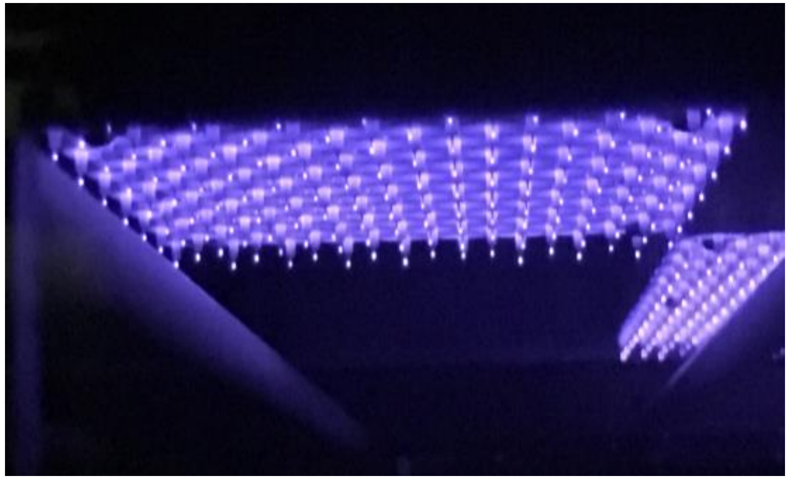
Novel Flux-free Technology with EA



- **Principle of Electron Attachment (EA) for hydrogen activation**
  - To dissociate H_2 molecules and form hydrogen anions
  - Air Products patented technology
  - Operable at ambient pressure and normal solder reflow temperatures using nonflammable mixtures of H_2 and N_2 (5% H_2 in N_2)
  - Completely residue free and environmentally benign



- When low-energy electrons (< 10 eV) collide with H_2 molecules, some are captured by H_2 molecules, producing atomic anions and neutral atoms
  - **Dissociative attachment:** $H_2 + e^- \rightarrow H_2^{-*} \rightarrow H^- + H$
  - **Direct attachment:** $H + e^- \rightarrow H^{-*}$
- The formed atomic hydrogen anions can be directed to the soldering surfaces for oxide reduction
  - **Surface de-oxidation:** $2H^- + SnO \rightarrow Sn + H_2O + 2e^-$



EA in operation

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Advantages of EA Based Reflow

- **Atomic hydrogen anion (H^-) formed under EA is a strong reducing agent**
  - Free of chemical bond
  - Good electron donor
- **EA environment is singly negative, thus extending the lifetime of H^-**
- **H^- automatically moves to the soldering surface driven by an electrical field**
- **Ambient pressure is more favorable than vacuum for forming H^- by EA**
- **N_2 is inert to EA and can assist in the formation of H^-**
- **EA flux-free process is completely residue free**

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Current Status of EA Based Fluxless Reflow

- Demonstrated concept and efficiency of EA technology for oxide removal
- Showed a potential of EA technology for a list of applications in electronics packaging: bump reflow, flip chip, die attach.
- Air Products has partnered with Sikama on building EA-enabled furnace for production-scale wafer bump reflow
- Alpha trials are being conducted at a R&D lab of Air Products
- Beta system being completed for production scale trials
- Various wafers received from key prospects have been processed through the furnace
    - Includes electroplated UBM bumped wafers and copper pillar wafers
- The reflowed wafers have passed standard quality inspections by the prospects providing the wafer samples

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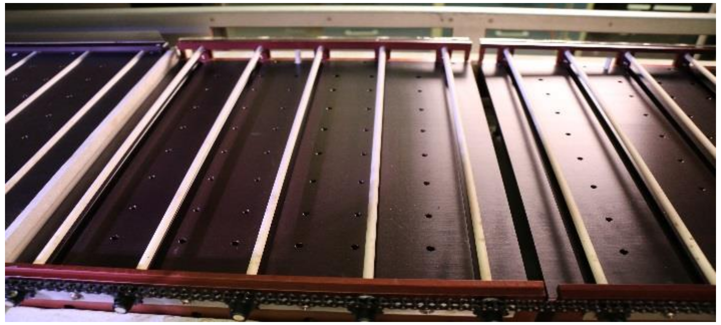
EA System Overview

- Roller system for wafer transportation (60 wafers/hour)
- Capable of handling wafers up to 300 mm in size
- Non-contact heating in combination with forced convection (ΔT ≤ 2℃)
- Reflow zone operable temperature up to 400℃
- Fully computer controlled furnace operation
- Foot print: 191.50” X 46.6”   (4.9 m x 1.2 m)

UP1200 EA-enabled furnace

Wafer moving on ceramic rollers



Non-contact heating

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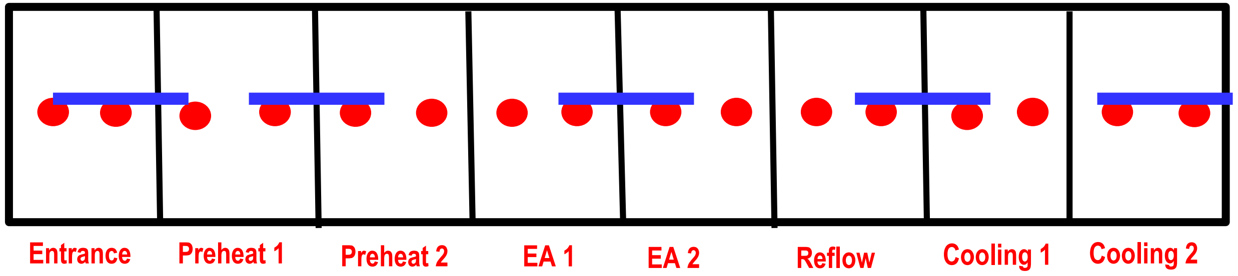
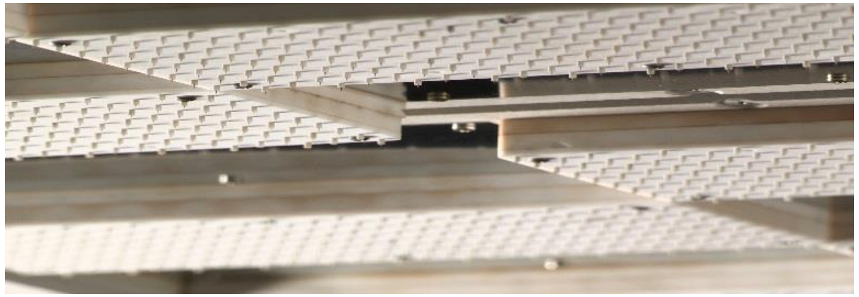
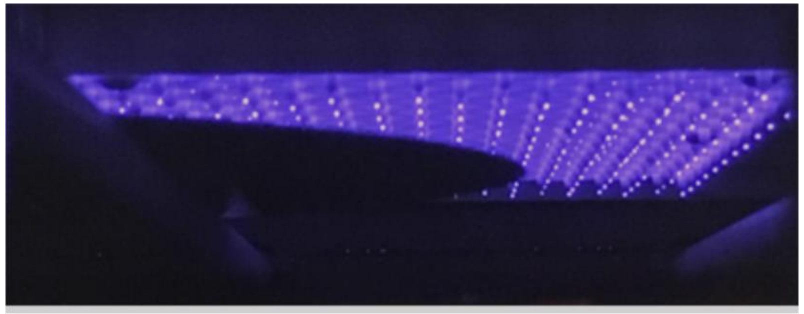
EA System Overview (con't.)

- 8 zone furnace with four sections using forming gas of 5% H2 in N2
  - 5 % H_2 in N_2 introduced into 2nd preheat section, two EA sections and reflow section
  - 100% N_2 for other zones
- O_2 level as low as 5 ppm are consistently achieved
- For each EA zone, an electron emission apparatus is mounted on the top side
- Before entering reflow zone, wafers are exposed to EA environment for oxide removal




Electron emission apparatus


Water moving into EA zone

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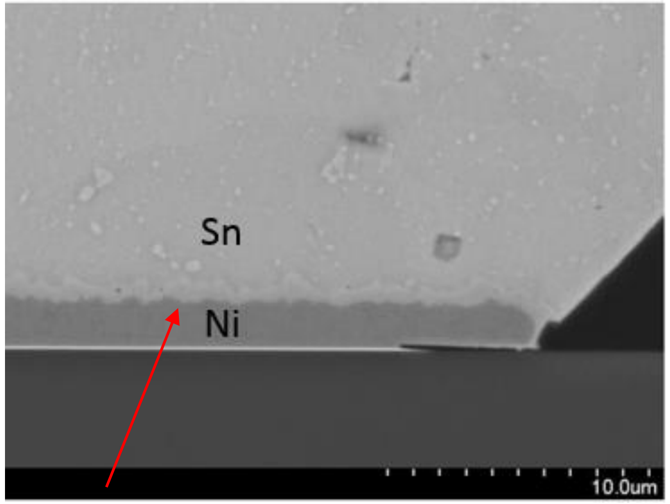
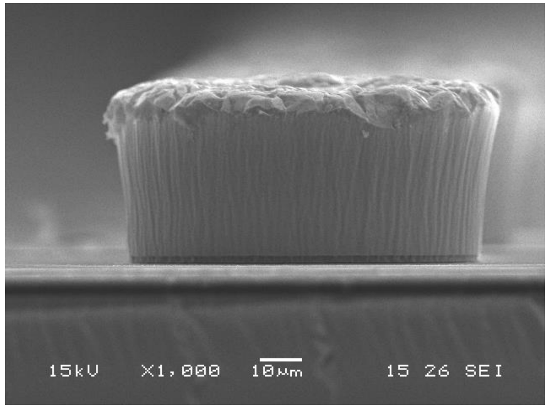
Mechanical Test – Individual Bump Reflow

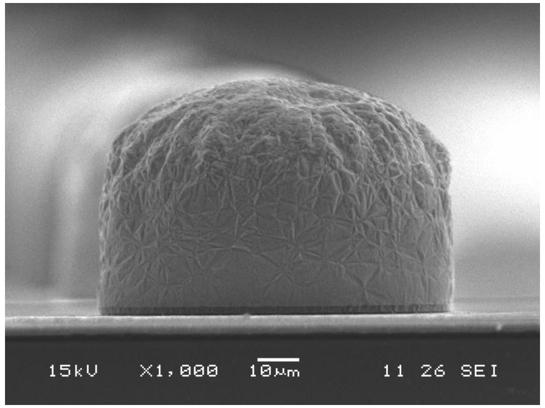
- **Bump reflow quality by EA reflow**
  - Acceptable IMC layer
  - Full bump shape conversion
    - Without EA, the reflowed bumps have a rough surface and incomplete shape change
    - With EA, the reflowed bumps are smooth and spherical, exhibits consistent diameter and height than that of flux-reflowed bumps



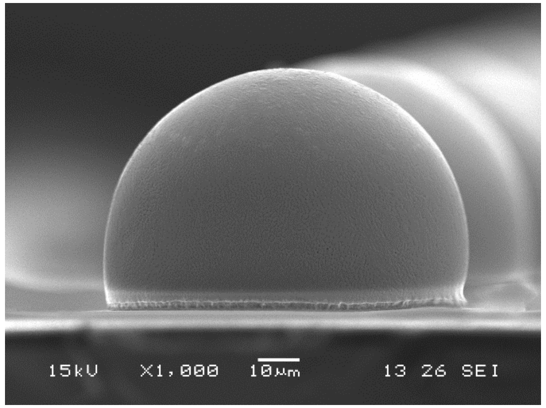
IMC layer of tin-based lead-free solder bump after reflow with EA



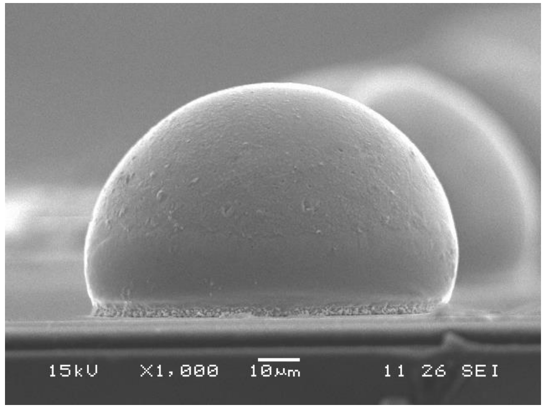
Before reflow



Reflow without EA



Reflow with EA



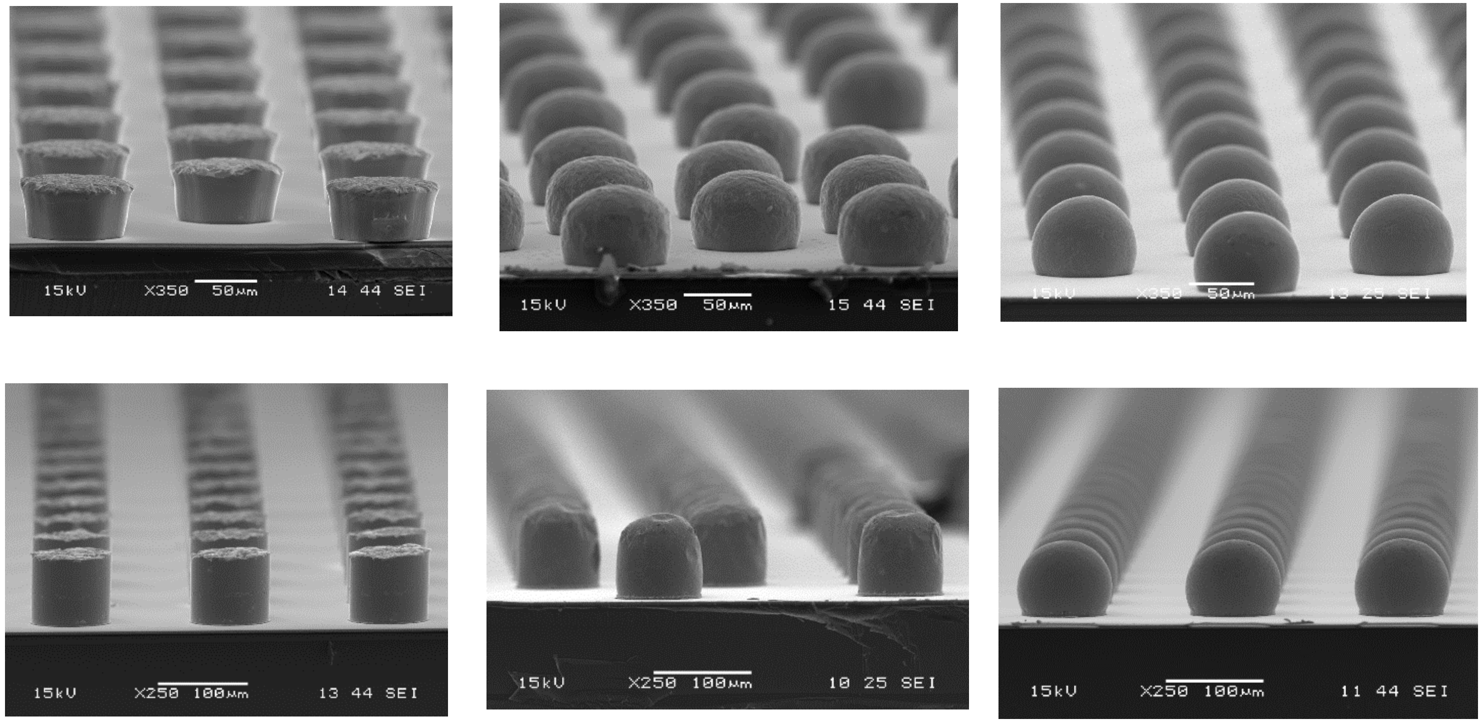
Reflow with flux

Mechanical Test – Array Bump Reflow

- **Bump reflow quality by EA reflow**
  - Without EA, the reflowed bumps have surface collapses and non uniform shape
  - With EA, solder bumps are completely reflowed with uniform bump height

Wafer #1

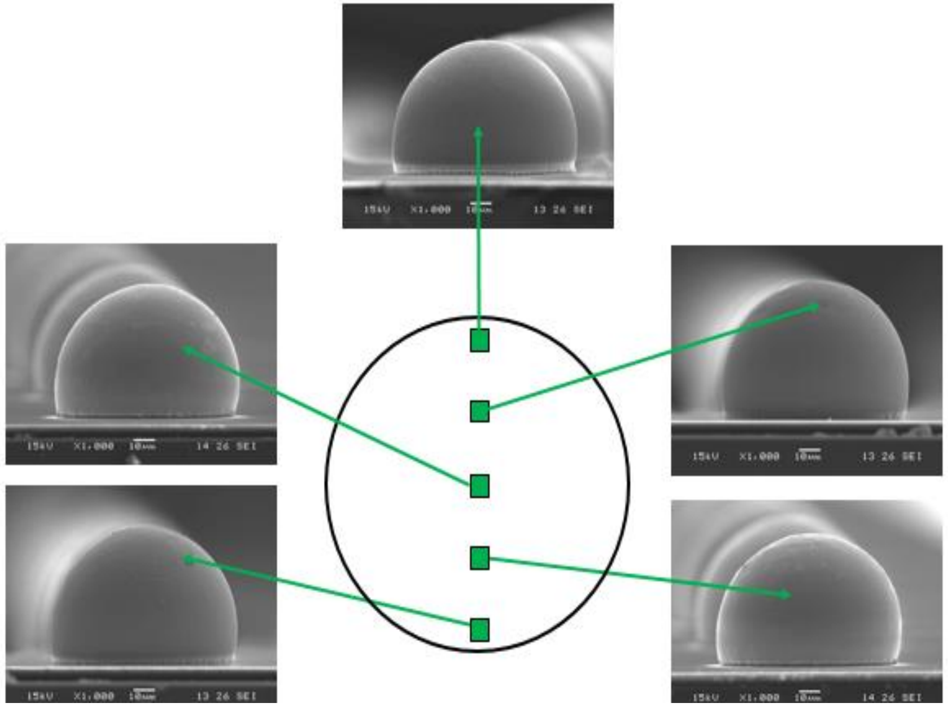
Wafer #2



Before reflow | Reflow without EA | Reflow with EA

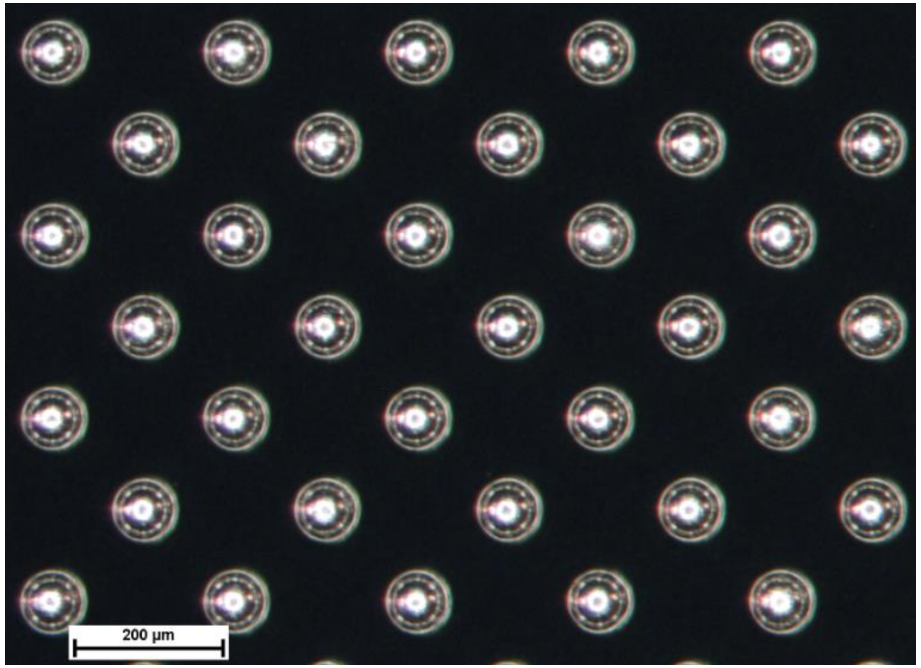
Mechanical Test – Bump Reflow Across 12" Width

- **Bump reflow quality by EA reflow**
  - Consistent bump uniformity across the width of a 12” moving wafer
- **Free of extra solder and foreign materials on wafer surface**



Wafer movement through furnace →

Uniform bump shape by reflow with EA



Clean wafer surface after reflow with EA

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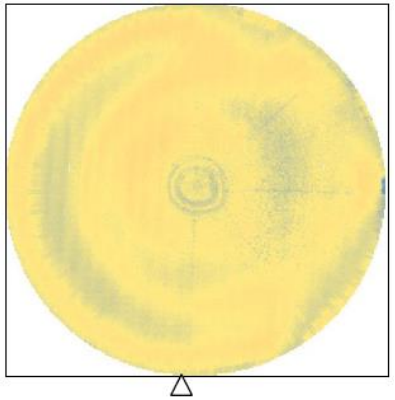
Mechanical Test - Full 8" Wafer Reflow

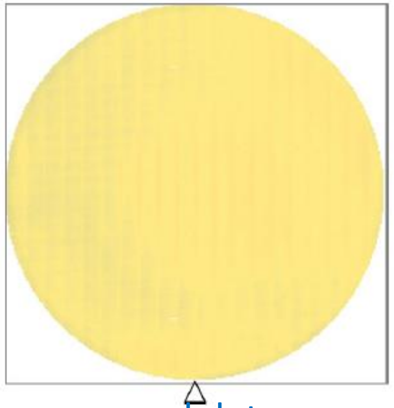
- **Customer standard quality inspections of full wafers with EA reflow**
  - AOI (Automatic optical inspection) shows that bump height and bump diameter across an 8” full wafer are within specifications
  - All shear failures are within solder bumps and shear strengths well exceed the criterion

Spec	62 ± 15 um
AVG BH	59.1um
Max BH	62.8um
Min BH	48.7um
BH Sigma	1.42um



Bump height distribution map and data

Spec	88 um +20%/-10%
AVG BD	90.2um
Max BD	91.9um
Min BD	88.0um
BD Sigma	0.47um



Bump diameter distribution map and data

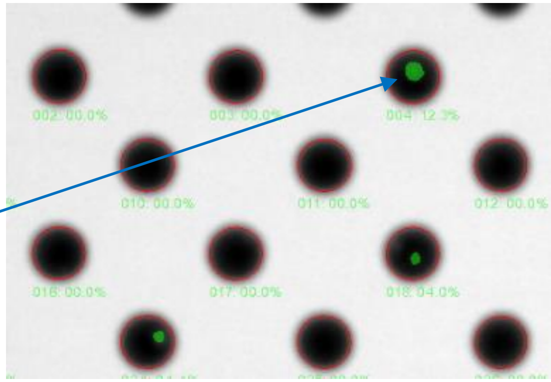
AVG	Max	Min
3.70	4.11	3.34

Spec>2 g/mil2

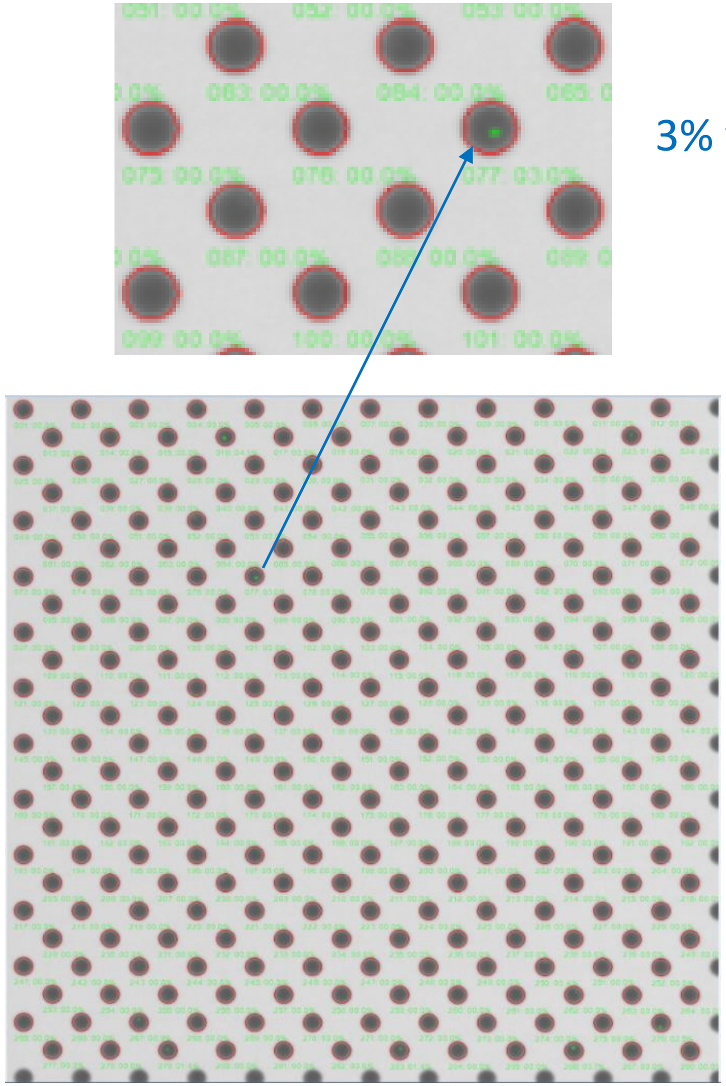
Bump shear failure and data

Mechanical Test - Full 8" Wafer Reflow

- **Customer standard quality inspections of full wafers with EA reflow**
  - Bump void inspection by x-ray passes criterion (< 8% of bump area)
    - Low number of bump void
    - Small void size (~3% of bump area)
- **Comparison**
  - Larger void number and size were found in the same type wafer reflowed with a flux



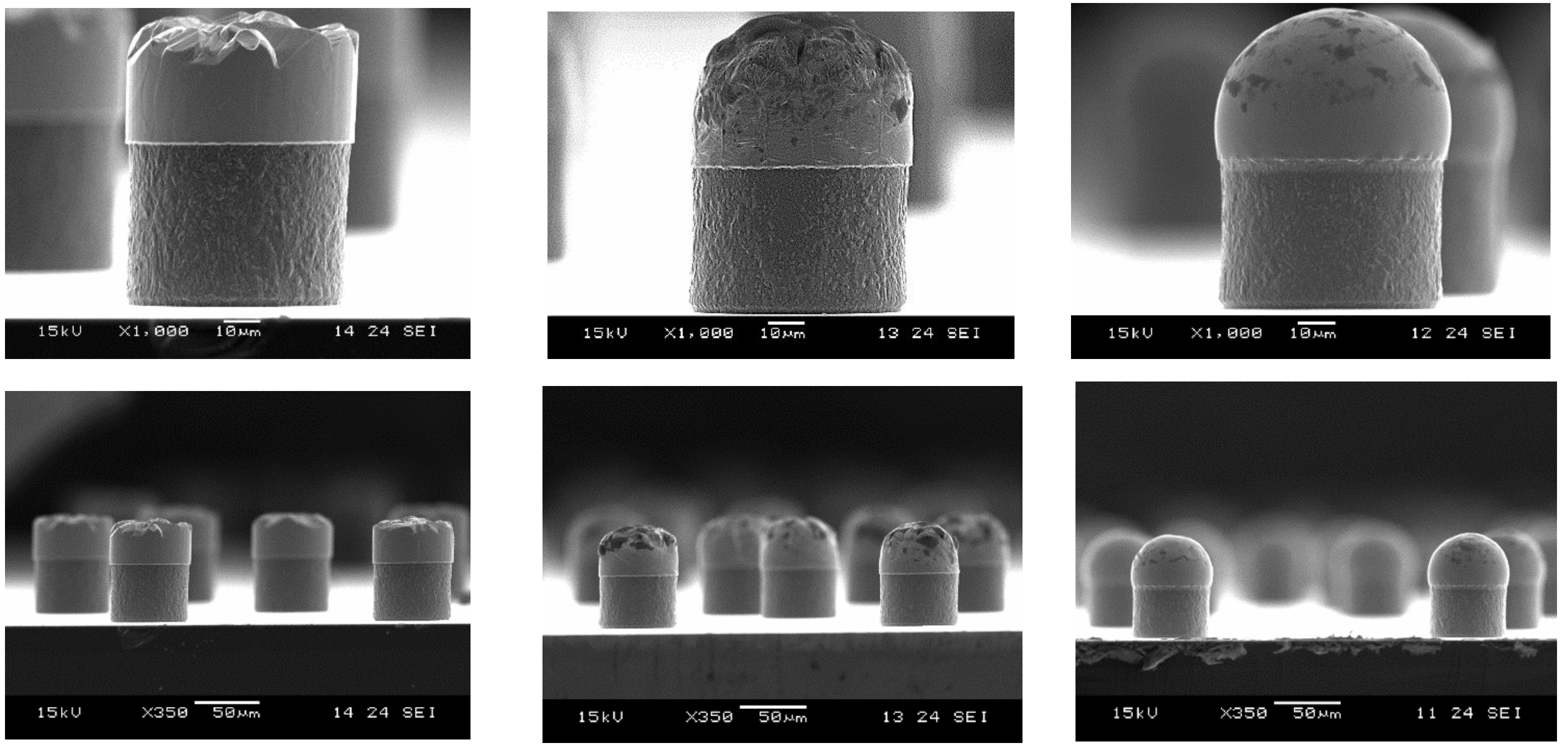
X-ray image for reflow with flux



X-ray image for reflow with EA

Mechanical Test – Mechanical Wafer A

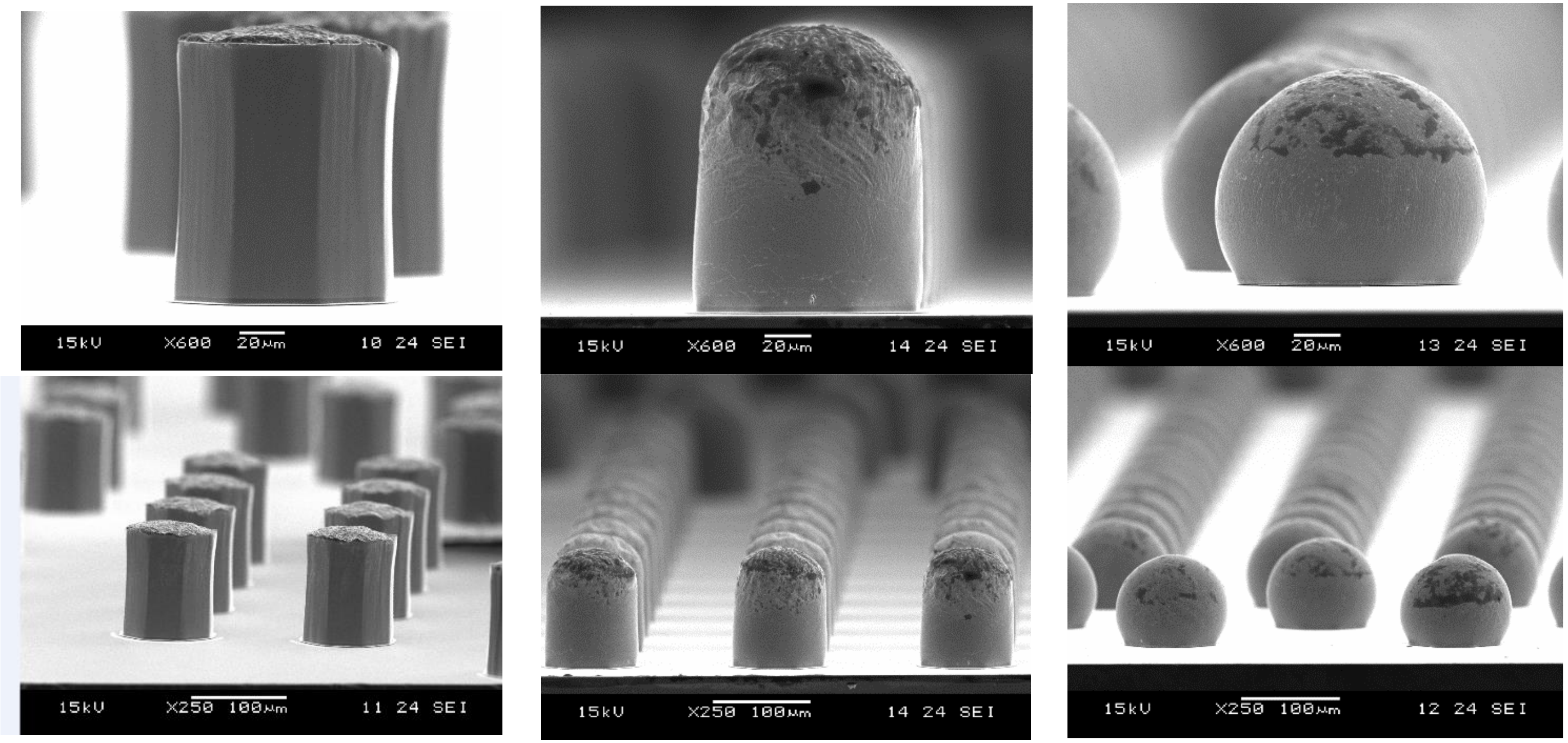
- Lead-free copper pillar bumps with 70 µm in diameter
- Completed bump shape conversion by EA-based reflow, equivalent to flux-based reflow



Before reflow Reflow without EA Reflow with EA

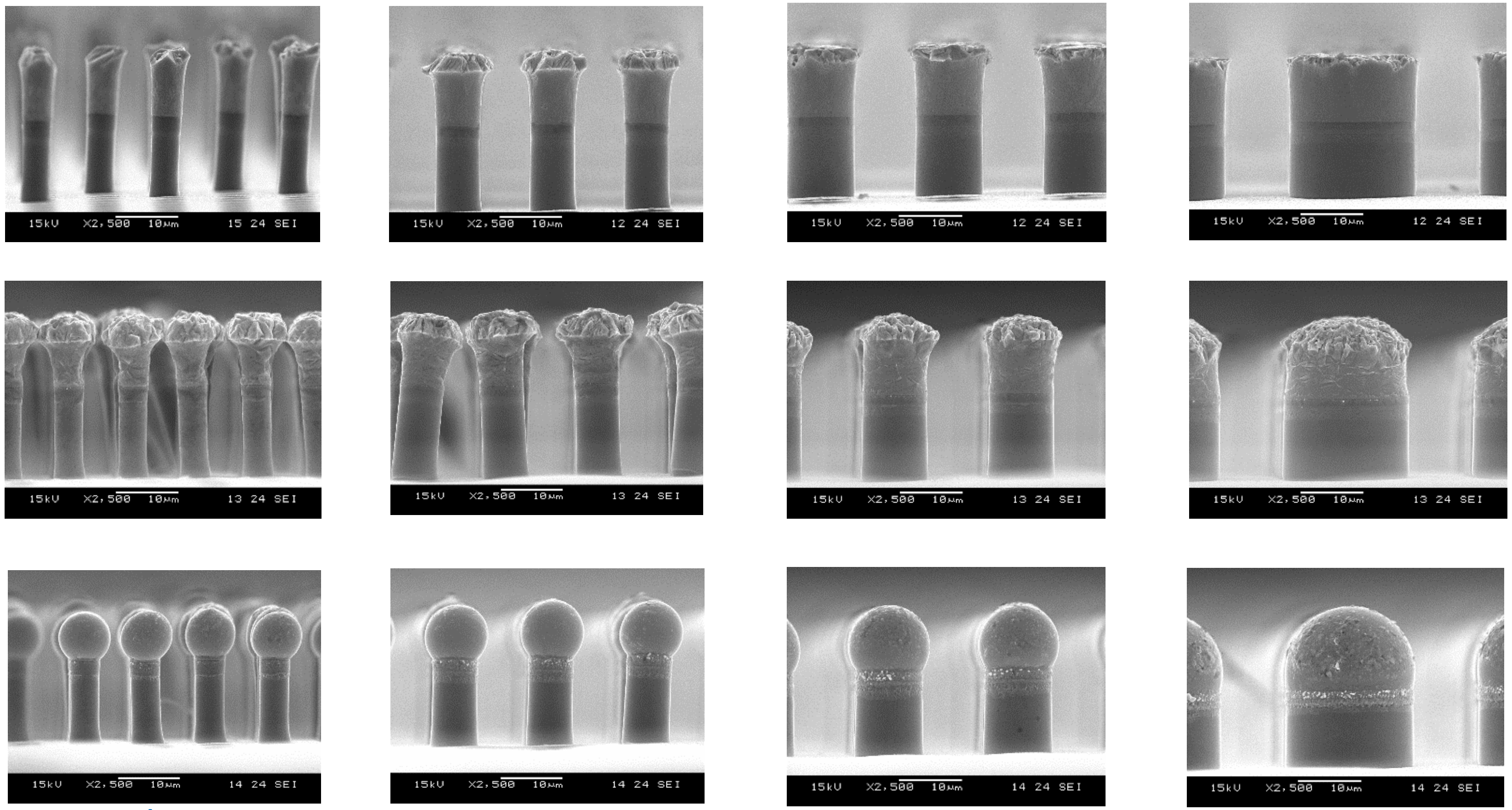
Mechanical Test – Mechanical Wafer B

- Lead-free UBM bumps with 100 µm in diameter
- Complete bump shape conversion by EA-based reflow



Before reflow | Reflow without EA | Reflow with EA

Mechanical Test – Mechanical Wafer C



Before reflow

Reflow without EA

Reflow with EA

6 µm diameter
6um pitch ???

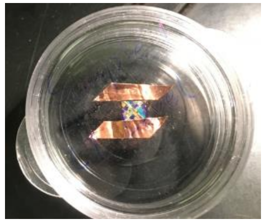
9 µm

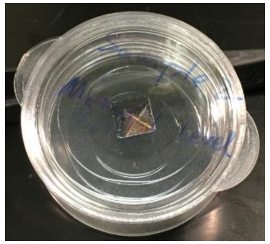
11 µm

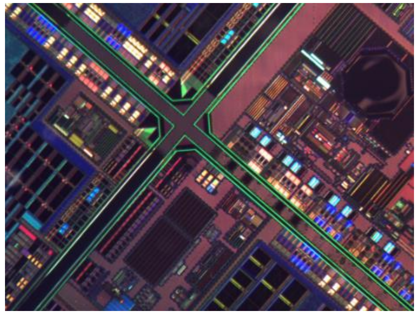
20 µm

Electrical Test – Transistor Level (SRAM at Contact Level)

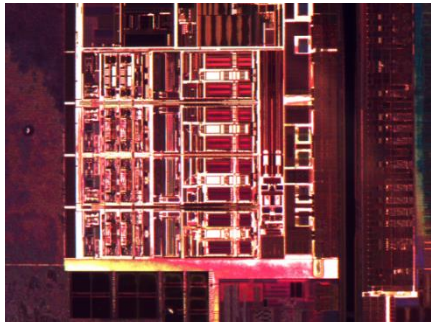
- **SRAM chips from a real product wafer at 28nm node**
  - Worse-case test (using almost naked transistors) to evaluate effect of EA plasma on functional devices
  - Passed functional dies through EA-enabled reflow furnace
  - Measured 12 SRAM transistors (2 bits) before and after EA reflow by Nano-probing



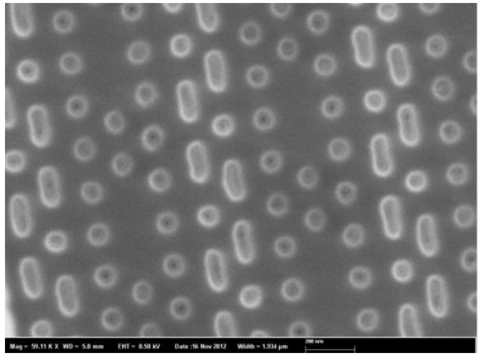




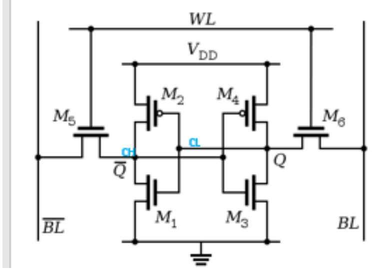
Die #1 --- Contact level

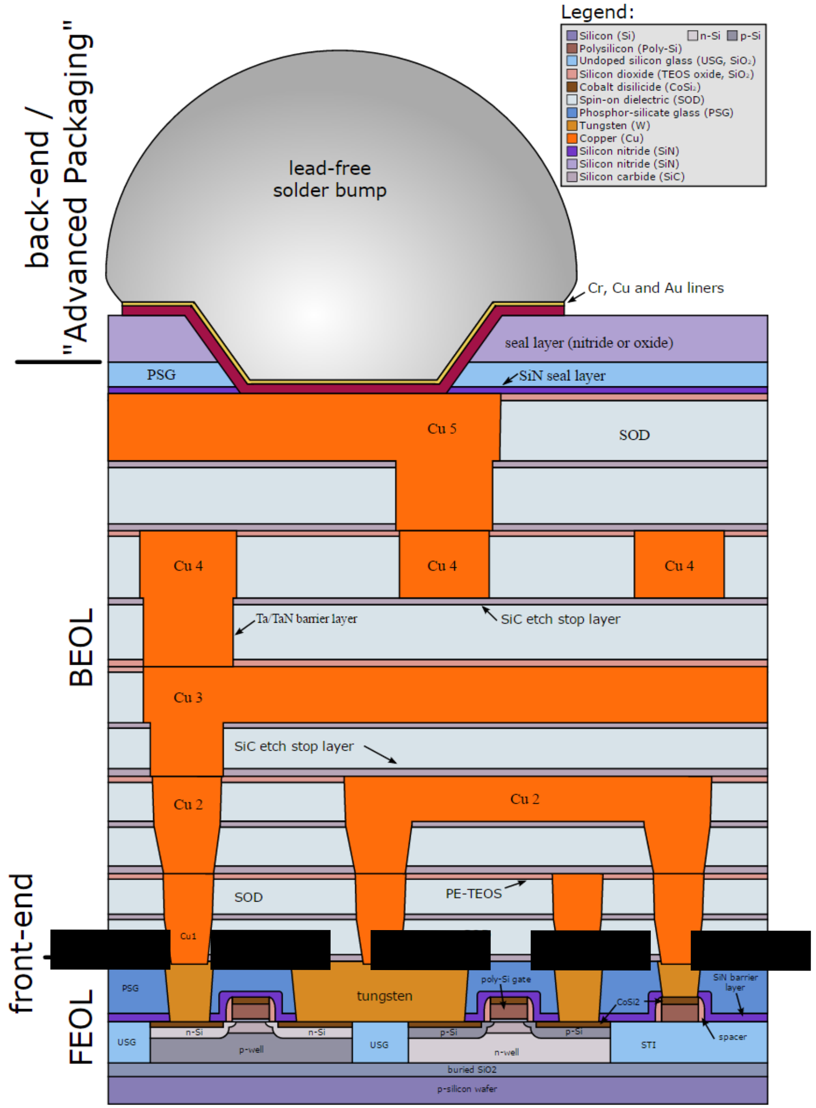


Die #2 --- Metal 1 level



SRAM – 6 Transistors





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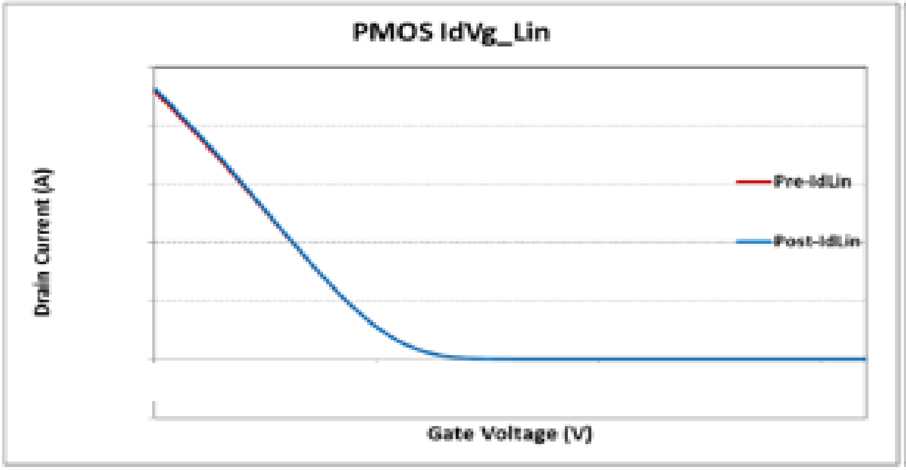
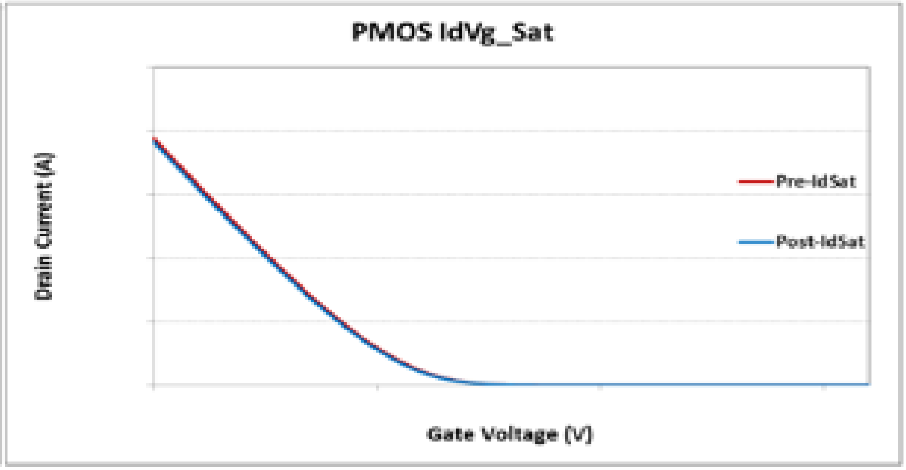
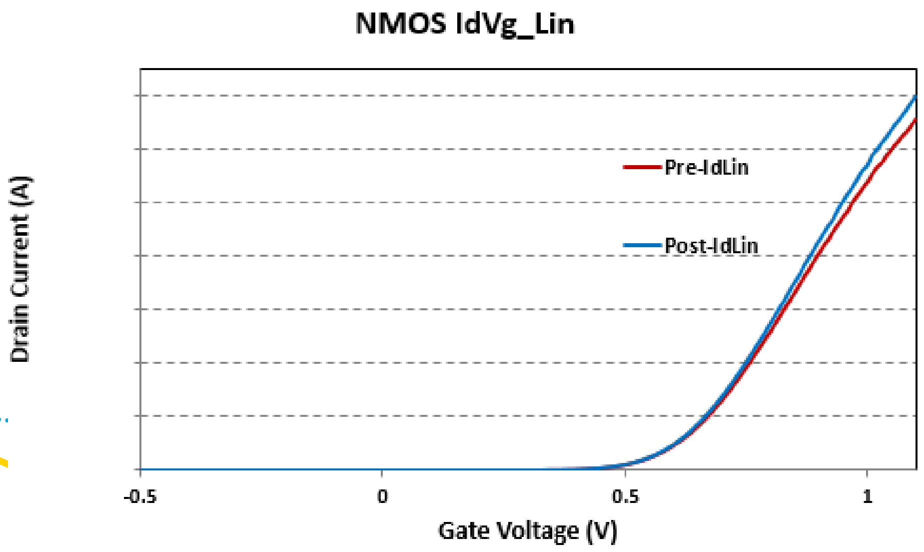
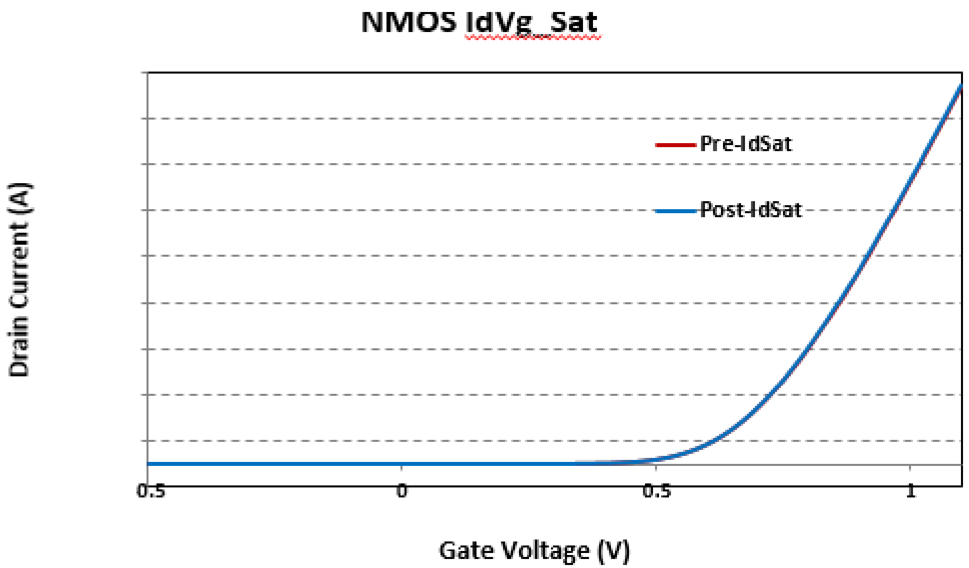
Electrical Test – Transistor Level (SRAM at Contact Level)

- IV curves (Id-Vg) overlay very well between pre- and post-EA exposures
- For both PMOS and NMOS, average change in Id-lin, Id-sat, Vt-lin, Vt-sat parameters are within 5% for all transistors (acceptable results).









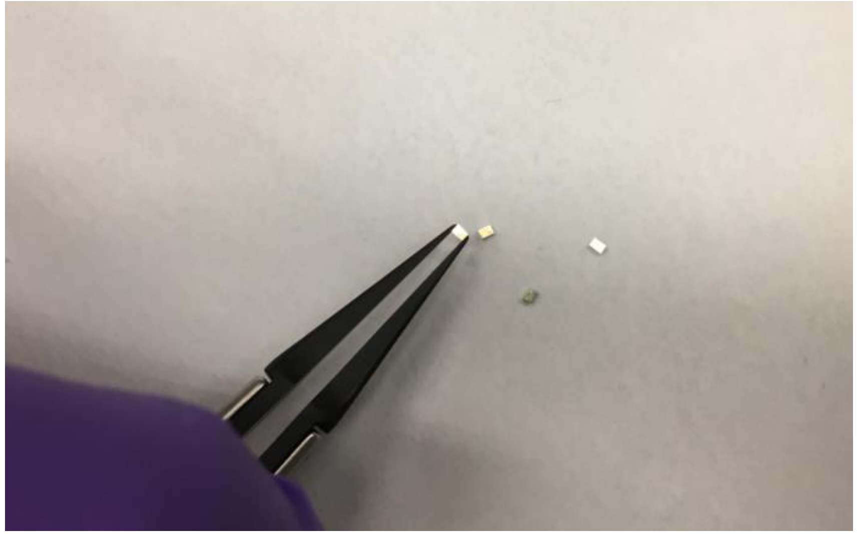
Electrical Test – Wafer Level – Functional Probed Wafer Test

- Functional probed solder bumped CMOS wafers were provided by a Major Semiconductor Company
- Two probed wafers were processed in the EA activated hydrogen reflow system
- Post EA processed probe testing showed insignificant changes to the device characteristics as compared to the pre EA process data
- Pre and post probe wafer testing was completed by the major semiconductor company
- Conclusion
  - EA activated hydrogen process had no effect on the electrical characteristics or functionality of the devices on the wafers.

Electrical Test – Chip Level - CMOS Amplifier (TI)

- Passing known-good-die (KGD) through EA-enabled reflow furnace
- All 30 EA exposed KGDs passed probe test, indicating no damage

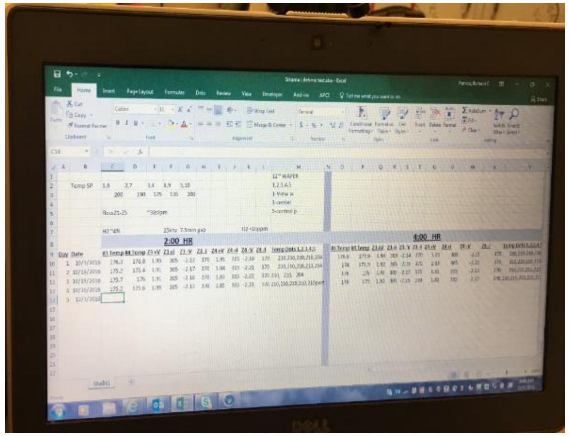
Tested 30 KGDs



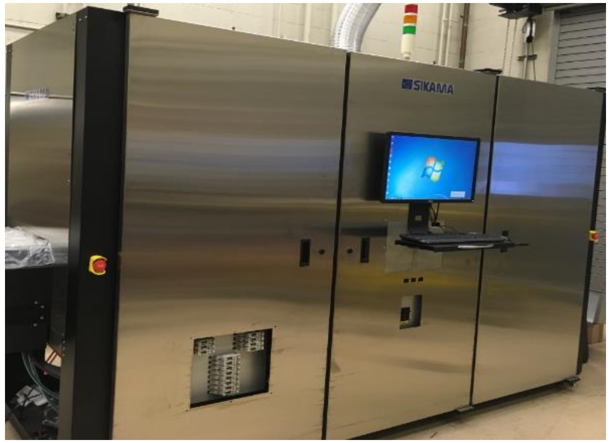
OPA 2333 CMOS operational amplifier

Alpha System Production Readiness

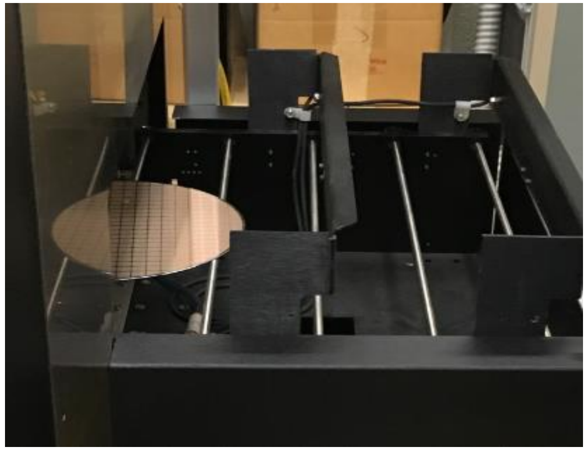
- Operating 8 hr/day, 5 days/week, daily start-up and shut-down
- Accumulated >1500 hours of successful operation in a production status
- Demonstrated system reliability and stability
  - Stable EA power
  - Reliable roller system for wafer transportation
  - Uniform temperature across a 12” wafer
  - Stable temperature at each zone



Operation record



EA-enabled furnace



Roller system

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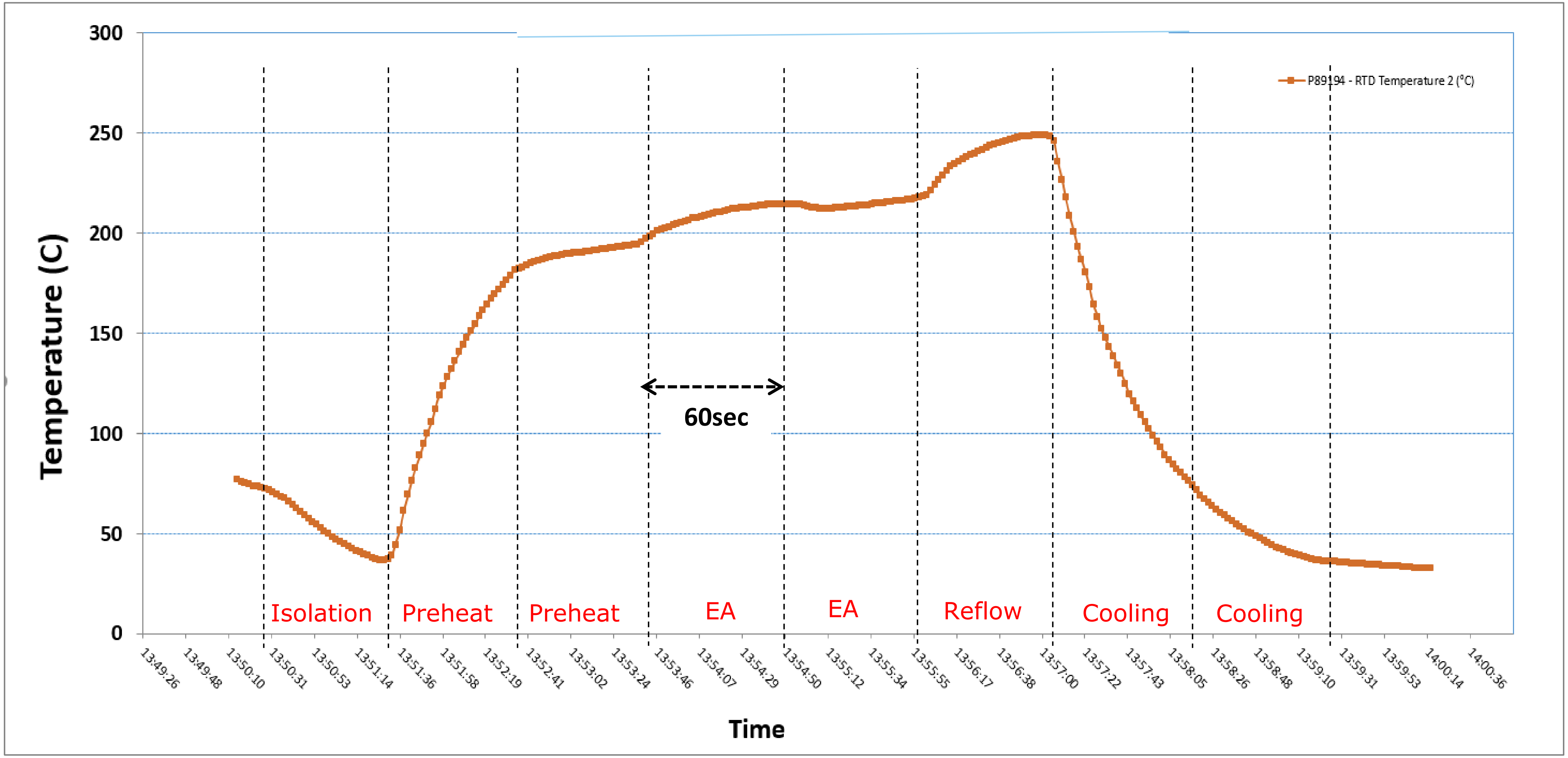
Furnace Temperature Profile



One Example of a Temperature Profile Across the Eight Zone Furnace

EA Comparing With Other Process

Comparison	Flux based	Formic Acid Based	EA Based
Organic Chemicals	Liquid flux	Gas flux	No
Reducing Capability	Ok in general cases	May not be sufficient	Good even for relatively low temperatures
Work Pressure	Ambient	Vacuum	Ambient
Parameter Control	Easy	More difficult	Easy
Equipment Versatility	Good	Limit	Good
Auxiliary equipment	Flux Coater	Bubbler with temperature and N_2 flow controls	H_2/N_2 gas distribution panel
Post Clean	Yes	Yes	No
Processing Cost	Relatively high	Relatively low	Lowest
Eq. Maintenance	Need	Need, 6hr/wk	No need
Maintenance Fee	General	High (Vacuum pump)	Low
Environmental Impact	Organic vapor and hazard wastes	Organic exhaust (need scrubber)	No
Other Operation and Quality Impacts	-Block N_2 flow by flux residues -Void formation by entrapped flux vapors -Reach limit for fine pitch bumps, e.g.: - Insufficient oxide removal - Incomplete post cleaning	- Vacuum plus step heating promotes: - solder splashing and beading - void formation by organic residue decomposition - Potential polyimide damage	- Ambient pressure plus controlled heating can: - prevent solder splashing and beading - minimize void formation by organic residues - High surface tension of molten solder can: - result in bigger bump height/improved mechanical properties - prevent solder migration to copper pillar - Roller system tolerates wafer warpage - Minimized bump damage by eliminating post cleaning

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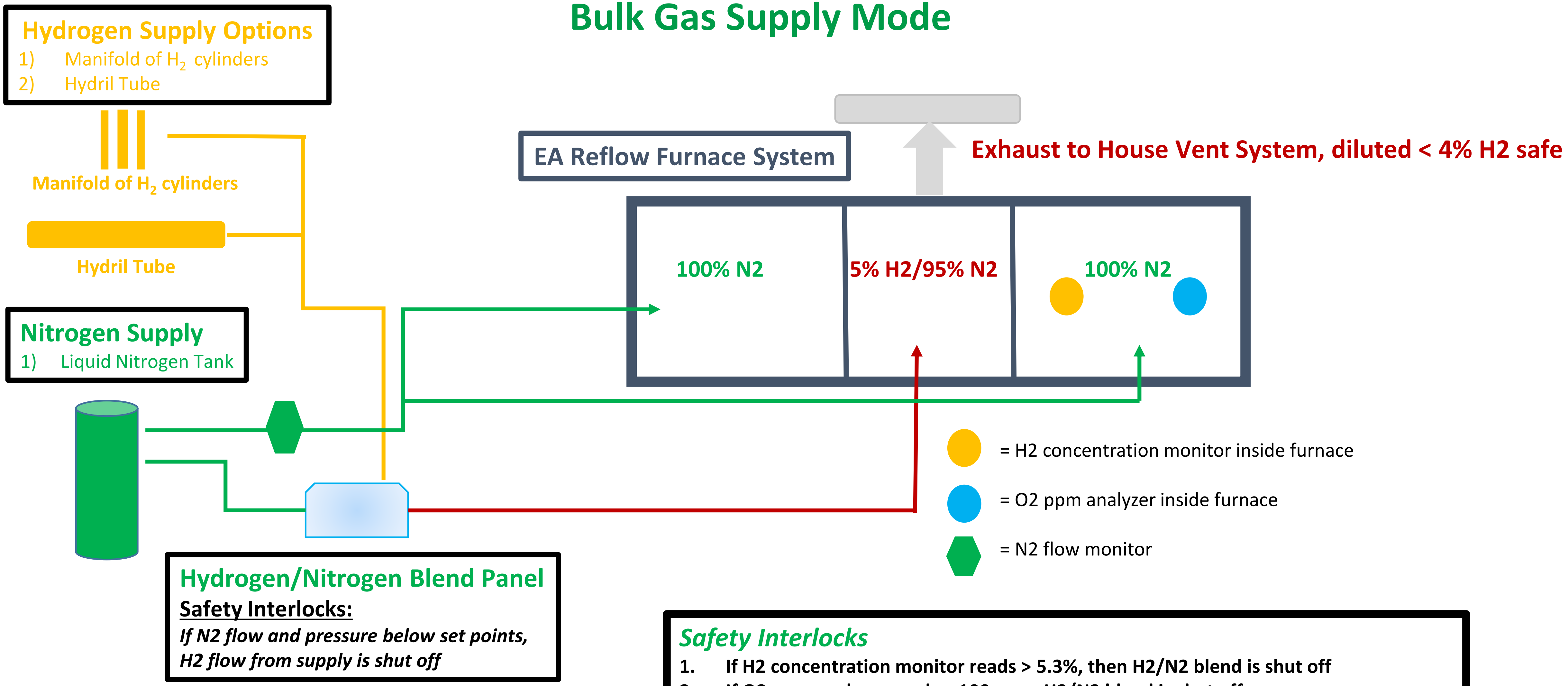
Cost of Ownership

Flux versus Activated H2 Technology

Assume 15,000 300mm wafer per month	Process of Record		EA technology
Material (flux/cleaning chemicals) Cost (US$/yr)	462,600		0
Gas Cost (US$/yr)	14,400		27,000
Equipment/asset Costs (US$/yr)	66,600		108,000
Power Cost (US$/yr)	21,600		12,000
Operation Cost (US$/yr)	12,600		21,600
Total Cost (US$/yr)	577,800		168,600
Cost Saving (US$/yr)			**409,200**
Material (flux/cleaning chemicals) Cost (US$/wafer)	0.08		0.00
Gas Cost (US$/wafer)	0.37		0.15
Equipment/asset Costs (US$/wafer)	0.12		0.60
Power Cost (US$/wafer)	0.07		0.07
Operation Cost (US$/wafer)	3.21		0.12
Total Cost (US$/wafer)	3.85		0.94
Cost Saving (US$/wafer)			**2.91**

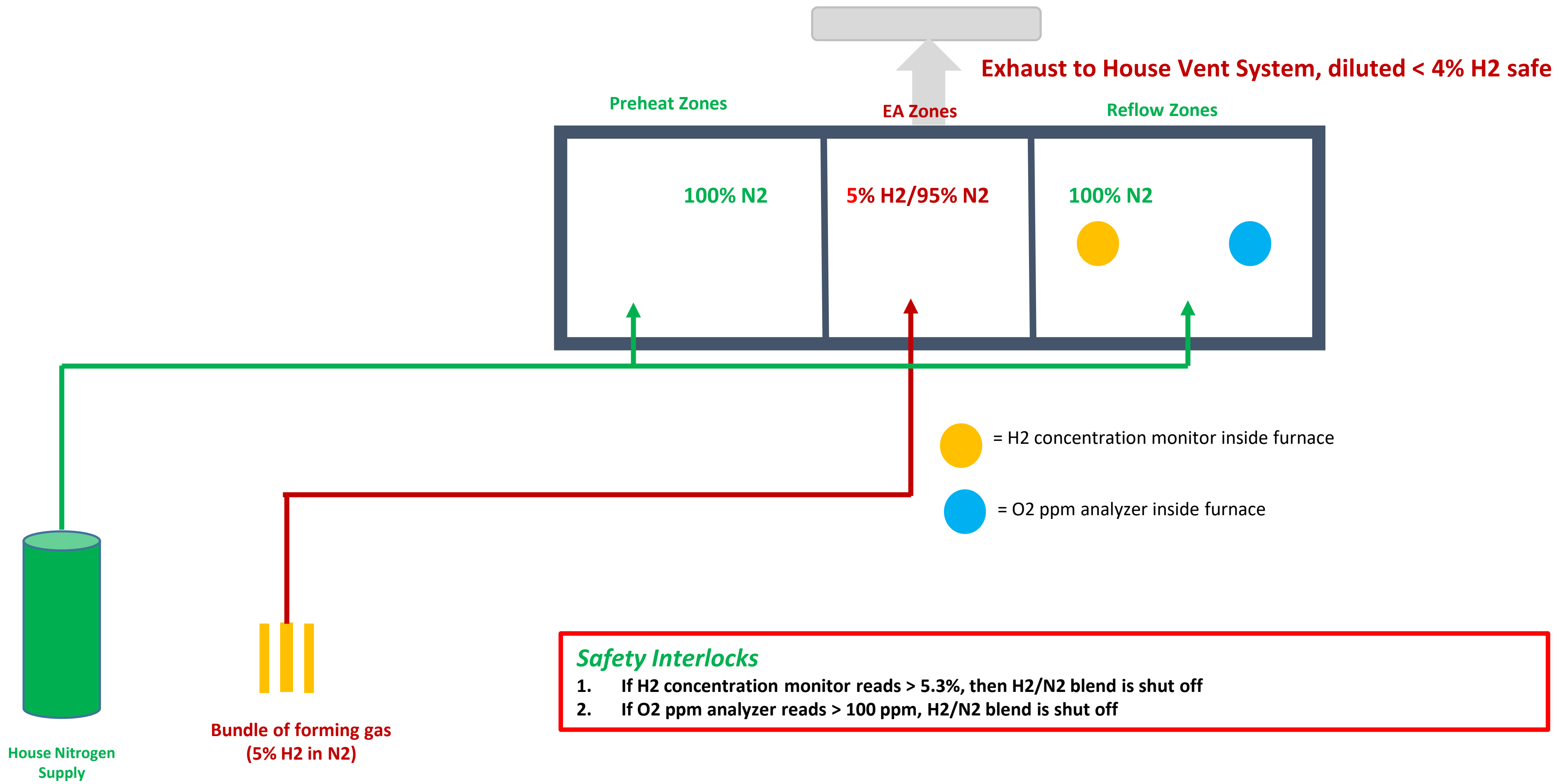
H2/N2 Gas Supply to Reflow Furnace
Bulk Gas Supply Mode



Safety Interlocks

1. If H2 concentration monitor reads > 5.3%, then H2/N2 blend is shut off
2. If O2 ppm analyzer reads > 100 ppm, H2/N2 blend is shut off
3. If N2 supply is interrupted (flow or pressure), H2/N2 blend is shut off

H2/N2 Gas Supply Mode
Premixed Cylinders



Safety Interlocks

1. If H2 concentration monitor reads > 5.3%, then H2/N2 blend is shut off
2. If O2 ppm analyzer reads > 100 ppm, H2/N2 blend is shut off

Hydrogen Safety in Handling H2/N2 Blended Gas

Safety

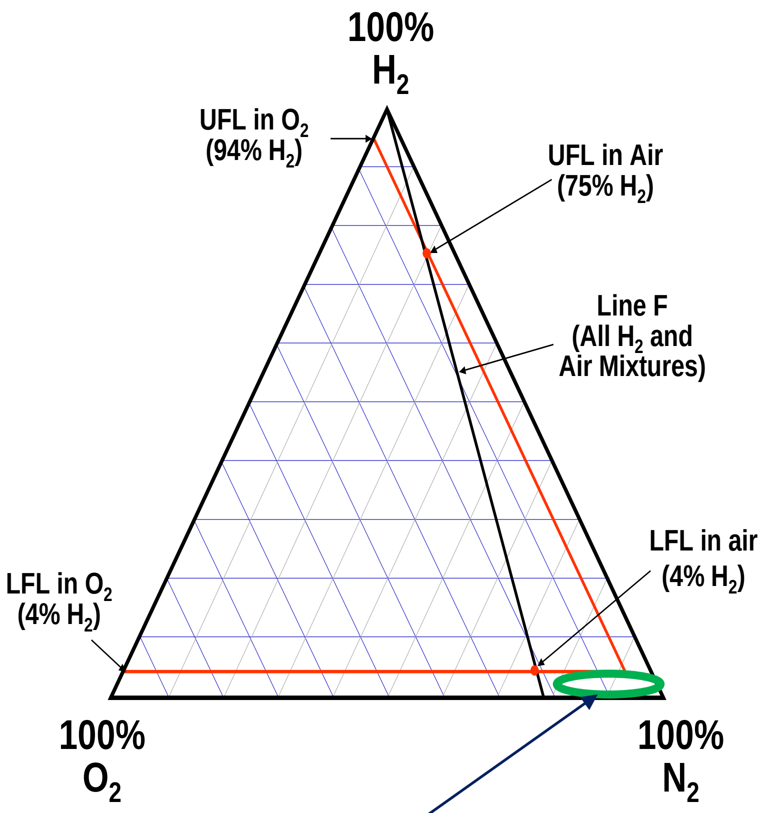
- The reason for the dilution of H2 by N2 is to keep H2 below 4 vol%, as this is the point above which the hydrogen can spontaneously combust.
- Depending on the gas supplier and EH&S rules, it may allow a maximum of either 5.0% or 4.0% H2 inside a furnace, to ensure the leaked gas within safety margin.
- In copper wire bonding systems, a 5% H2 in N2 is commonly used.
- 100% H2 furnaces are used around the world in different processes.
- There are soldering processes where 10% or 20% H2/N2 forming gas is in use.
- >5% H2/N2 can be safely used, but you have to be careful when using it with the appropriate safety interlocks.

Gas Supply

There are two practical ways of supplying gas for forming gas-based soldering processes:

Mixing H2 and N2 in a special blending panel. This process makes a very "clean" forming gas that will have optimal reducing properties. Usually, the N2 source is from vaporized cryogenic N2, and the H2 is from a cylinder or "tube"-based sources.

Cylinder supply. A single cylinder, or a manifold bank of cylinders may be used to provide the H2/N2 gas as a mixture.



Air Products EA technology uses 5% H2 in N2 which is below the Lower Flammable Limit (LFL)

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Conclusion

- **AP/Sikama team has completed in designing, building, testing, and qualifying the EA-based flux-free solder reflow system. The system can provide a production-ready process solution to IC packaging industry.**

- **System hardware tests and actual mechanical and electrical samples have met specifications.**
  - System is capable of operating in a reliable and stable condition
  - EA-based reflow is superior than flux-based reflow, especially for single digit µm bumps
  - Electrical studies of functional devices after EA reflow showed negligible effects on device reliability.
  - The EA-enabled production-scale furnace is working well

- **EA technology offers the following benefits for wafer bump reflow:**
  - Enhanced bump reflow quality (no flux-induced solder voids and wafer contaminations)
  - Improved productivity (in-line process, no need for post wafer cleaning and furnace down time cleaning)
  - Reduced cost of ownership (no need for cleaning equipment, solution, labor work, and flux)
  - Improved safety (no flux exposure, using a non-toxic and non-flammable gas mixture)
  - No environmental issues (no organic vapors, hazard residues, and CO_2 emission)

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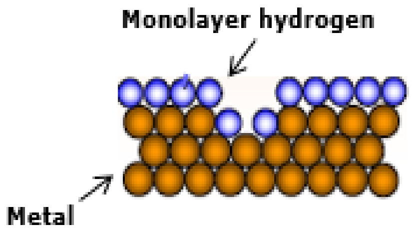
Future development programs

- Surface cleaning via activated H2 buffering
  - Removing oxides via EA activated H_2 in N_2
  - Forming a monolayer hydrogen on metal surface to inhibit re-oxidation
  - Initial results have demonstrated good results
    - Result shows around two to three days buffering effect based on spreading tests



Without EA-Clean

EA-cleaned with acceptable air exposure time

- Objective is to pursue IC packaging applications (flip chip, die attach, thermal compression bonding…..)

Future development programs

- **C2W and Flip Chip Assembly**
  - Using Activated H_2 buffering process
    - Whole wafer bump oxide removal
    - Substrate oxide removal
    - On line or off line processes
    - Place chip to substrate, TCB tack, then reflow in N_2 or forming gas atmosphere
- **Cu to Cu Thermocompression Bonding**
  - Using Activated H_2 buffering process
    - Cu pillar , no solder cap, remove copper oxide
    - Substrate oxide removal
    - On line or off line processes
    - Place chip to substrate, TCB tack, then reflow in N_2 or forming gas atmosphere
- **2.5D and 3D assembly**
  - Same as above

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Thank you